

Spécialité de Master « Optique, Matière, Paris »

Stage de recherche (4 mois minimum, à partir de début mars)

Proposition de stage (ne pas dépasser 1 page)

Date de la proposition :

Responsable du stage / internship supervisor:			
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Code d'identification :	UMR9001	Organisme :	CNRS/Univ. UPSaclay
Site Internet / web site:	https://toniq.c2n.universite-paris-saclay.fr/en/activities/sandwich/		
Adresse / address:	avenue de la Vauve - Palaiseau		
Lieu du stage / internship place:	Palaiseau		

Titre du stage / internship title: Hybrid III-V semiconductor on SOI optoelectronic devices
Photonic devices play a crucial role in the domain of information and communication technology, due to their ability to bring efficient solutions to data transmission and processing. Tremendous development, through optical fibres backed by related devices and circuits composed of light sources, optical amplifiers, wavelength multiplexers, photodetectors, etc, have greatly revolutionized communication in general. As a necessary evolution, attention is now being directed to optical datacom and computercom with an emphasis on the conception of power efficient ultracompact optoelectronic components. In photonics, the challenges which we face today, swirls around providing together the necessary active and passive functionalities fully integrated into a chip. These functionalities are, among others, light emission and amplification, filtering, wavelength routing ((de)multiplexing), detection or switching. Because all of these functionalities have to comply with ultra-compactness and low-loss circuitry while maintaining low cost production in CMOS fabs, few materials can pretend to fit in. In this context, Silicon on insulator (SOI) photonics, enhanced by III-V semiconductors is a key technology combining the best of both materials leading to a highly versatile hybrid photonics platform which opens the way to large scale photonic integration. During the last years, in my research team, we have taken forward this domain to the nanophotonic world by demonstrating III-V on SOI active devices based on planar photonic crystals (PhCs) to address the issues of compactness and power efficiency. Indeed, planar PhCs which consist of wavelength scale arrangements of holes (typ. radius~100nm), drilled into a semiconductor thin slab enable a quasi-extensive control of the electromagnetic field confinement and propagation. They have demonstrated over the last decade their capacity to shelter extremely efficient nonlinear interactions exploitable for low threshold laser emission, all-optical switching, etc... The proposed project aims at building a new panel of hybrid III-V on SOI optical devices with performance beyond the state of the art in terms of footprint, power efficiency and speed, to meet the stringent requirements for on-chip optical interconnects. The targeted components will be electrically driven nanolaser [1], an optical amplifier and a memory [2]. The student will be required to focus on the design, fabrication, and experimental aspects with continuous feedbacks "loops" between all these different aspects. This multi-task work is possible with the remarkable facilities and resources of C2N. [1] G. Crosnier, R. D. Sanchez, S. Bouchoule, P. Monnier, G. Beaudoin, I. Sagnes, R. Raj, F. Raineri, Nature Phot. 11 , 297 (2017) [2] S. Fitsios, T Alexoudi, A Bazin, P Monnier, R Raj, A Miliou, GT Kanellos, N Pleros, F Raineri, Opt. Express 24 , 4270-77 (2016)
Toutes les rubriques ci-dessous doivent obligatoirement être remplies

Ce stage pourra-t-il se prolonger en thèse ? Possibility of a PhD ? : oui			
Si oui, financement de thèse envisagé/ financial support for the PhD: ERC project			
Lumière, Matière, Interactions	x	Lasers, Optique, Matière	x

Fiche à transmettre (fichier pdf **obligatoirement**) sur le site <http://stages.master-omp.fr>